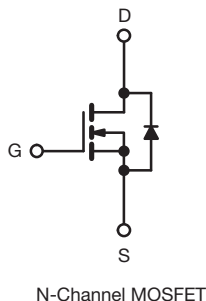


E Series Power MOSFET

Thin-Lead TO-220 FULLPAK



FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ max. (Ω) at 25 °C	$V_{GS} = 10$ V	0.6
Q_g max. (nC)	48	
Q_{gs} (nC)	6	
Q_{gd} (nC)	11	
Configuration	Single	

ORDERING INFORMATION

Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free	SiHA6N65E-E3
Lead (Pb)-free and halogen-free	SiHA6N65E-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C) ^e	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	18	
Linear derating factor		0.63	W/°C
Single pulse avalanche energy ^b	E_{AS}	56	mJ
Maximum power dissipation	P_D	31	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dV/dt	$T_J = 125$ °C	V/ns
Reverse diode dV/dt ^d			
Soldering recommendations (peak temperature) ^c	For 10 s	300	°C
Mounting torque	M3 screw	0.6	Nm

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 2$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature

**THERMAL RESISTANCE RATINGS**

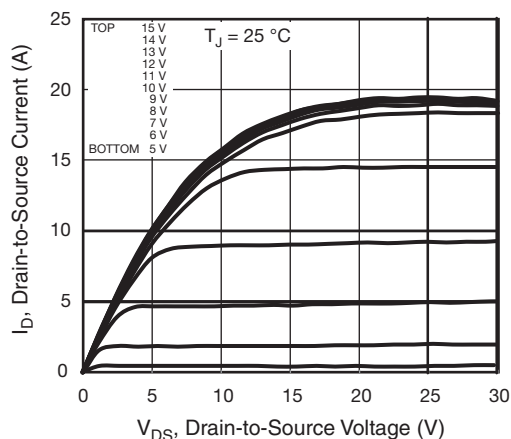
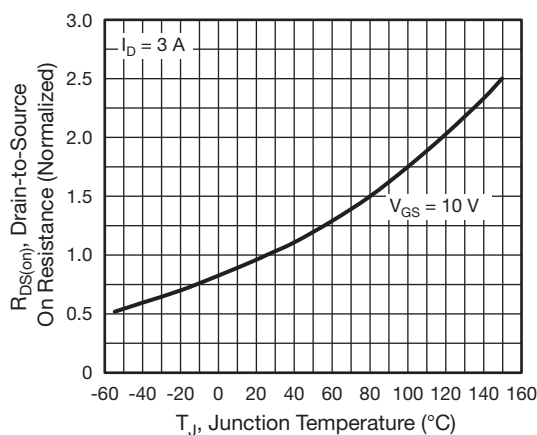
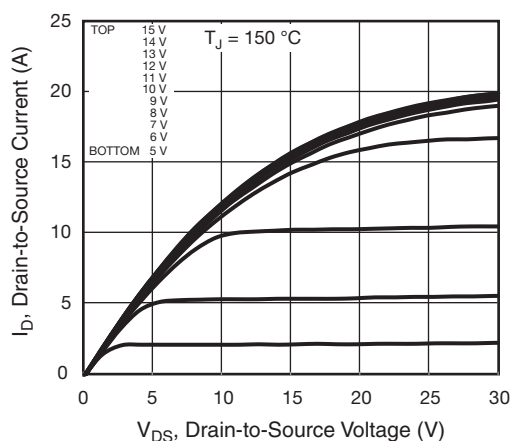
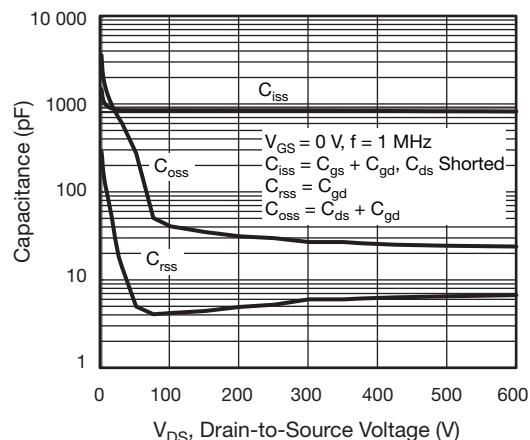
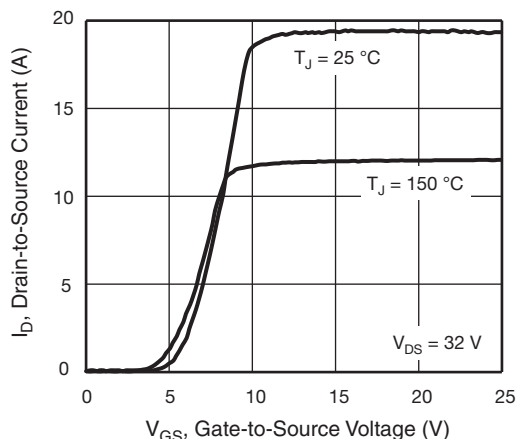
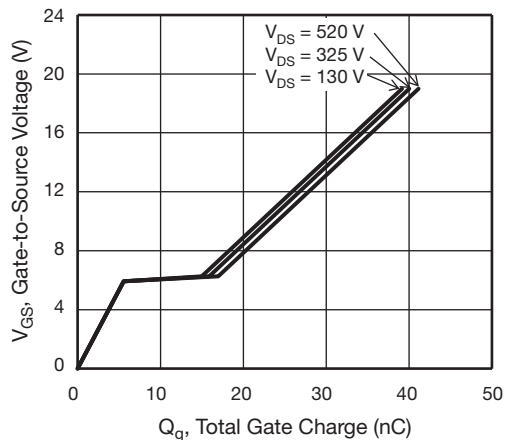
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	43	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	3.1	4.0	

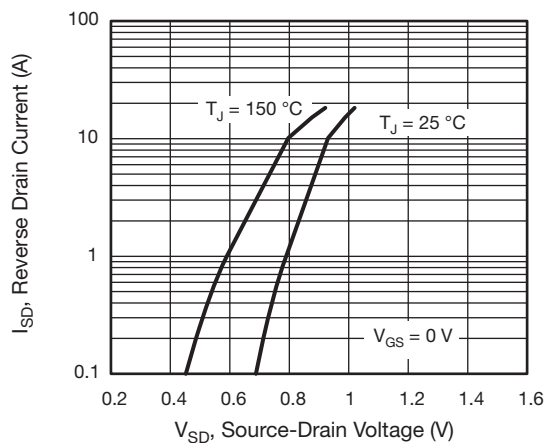
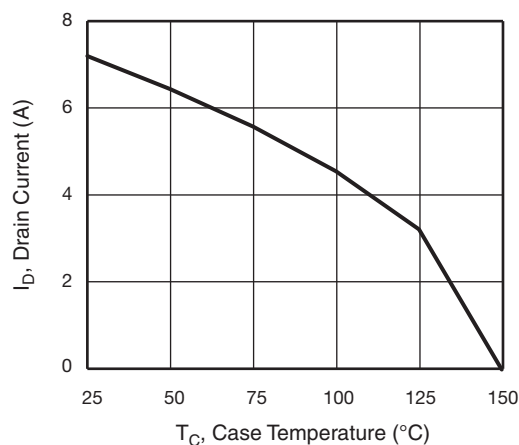
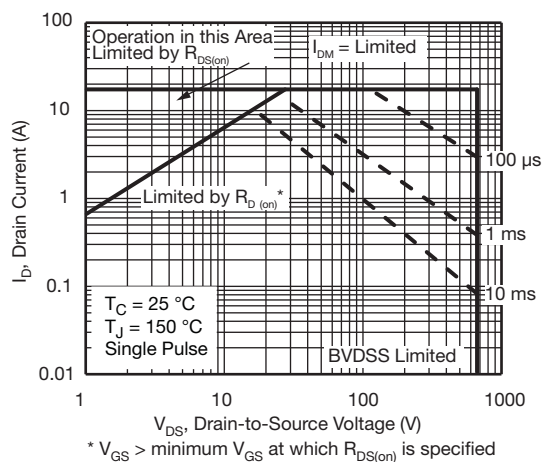
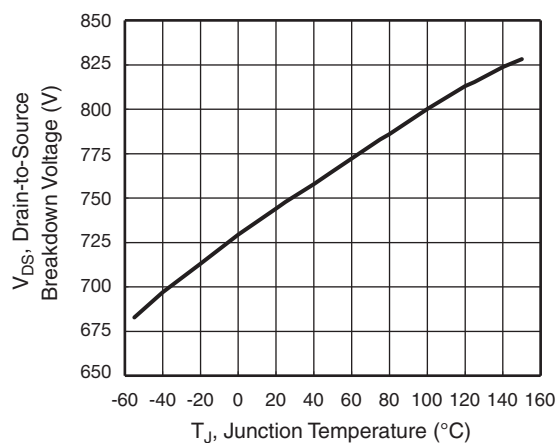
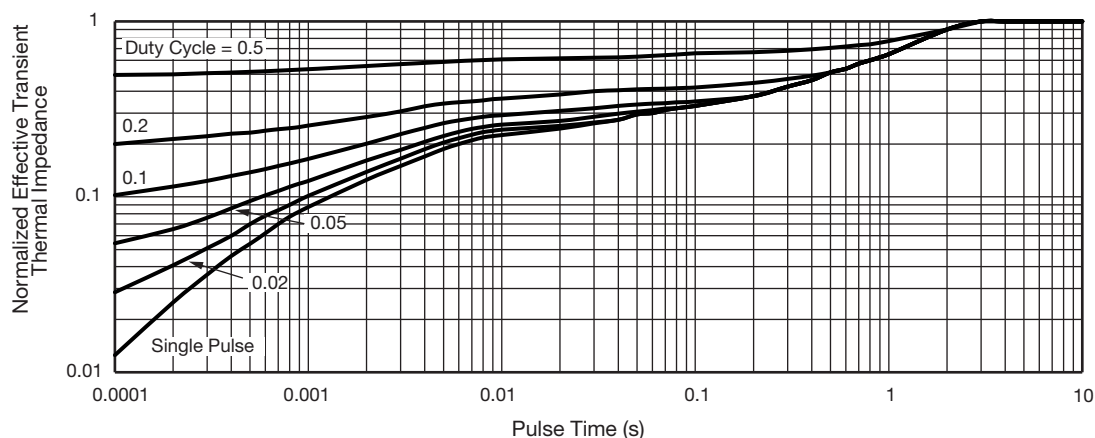
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

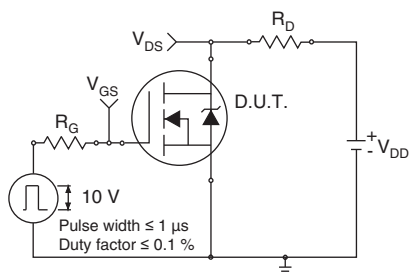
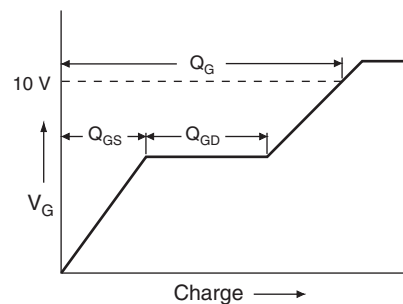
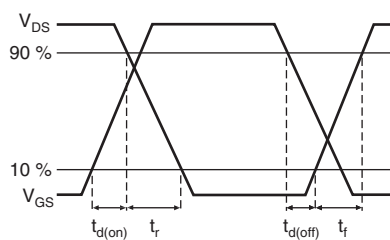
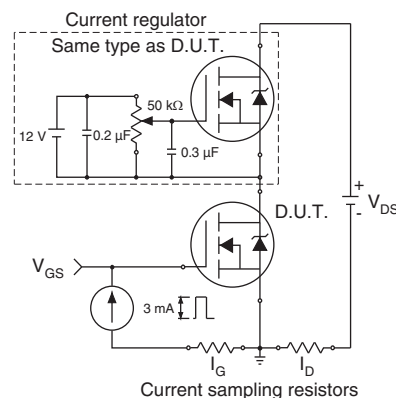
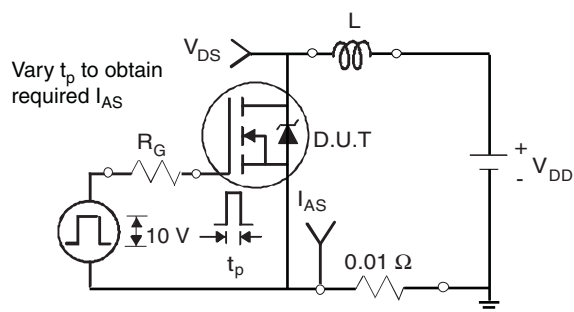
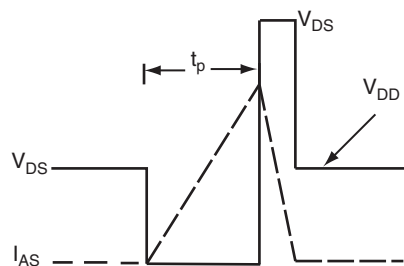
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	650	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.73	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 520\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$	-	0.5	0.6	Ω
Forward transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 3\text{ A}$	-	2	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	410	820	1640	pF
Output capacitance	C_{oss}		20	40	80	
Reverse transfer capacitance	C_{rss}		2	4	8	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}$, $V_{GS} = 0\text{ V}$	-	36	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$		-	117	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$, $V_{DS} = 520\text{ V}$	-	24	48	nC
Gate-source charge	Q_{gs}		-	6	-	
Gate-drain charge	Q_{gd}		-	11	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 520\text{ V}$, $I_D = 3\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	14	28	ns
Rise time	t_r		-	12	24	
Turn-off delay time	$t_{d(off)}$		-	30	60	
Fall time	t_f		-	20	40	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain	0.4	1.4	2.7	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	7	A
Pulsed diode forward current	I_{SM}		-	-	18	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 3\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.83	1.3	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	118	237	474	ns
Reverse recovery charge	Q_{rr}		-	2.2	-	μC
Reverse recovery current	I_{RRM}		-	16	-	A

Notes

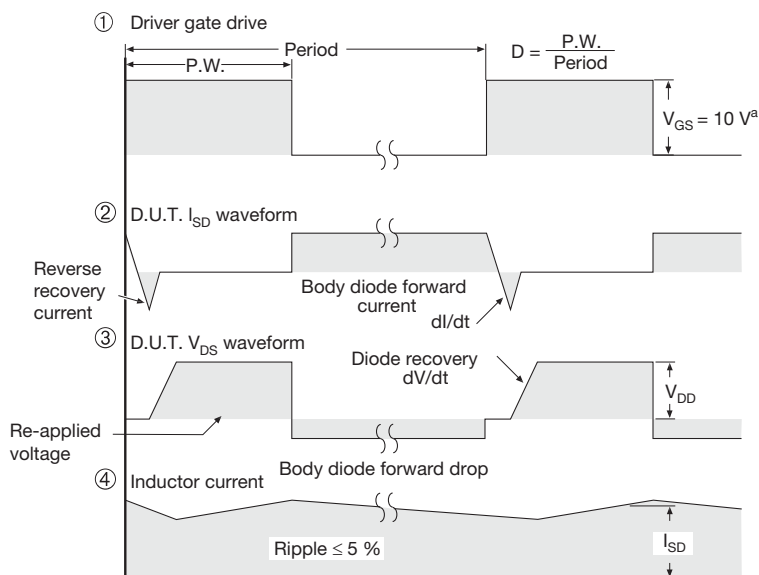
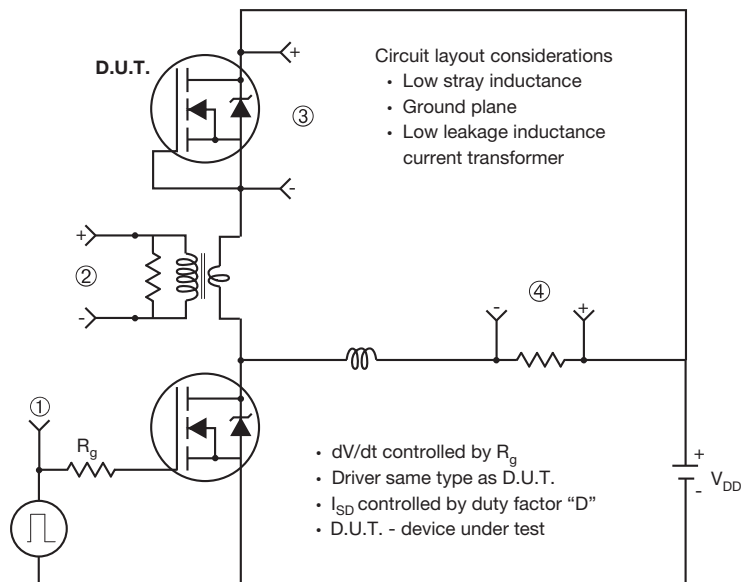
- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Temperature vs. Drain-to-Source Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit



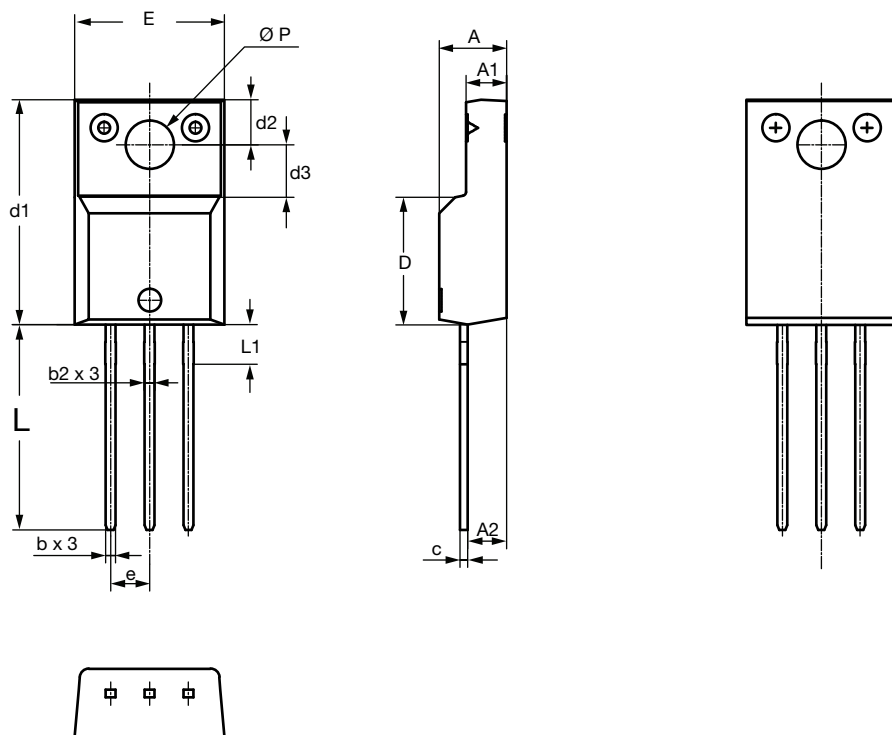
Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.40	2.80	0.094	0.110
b	0.60	0.80	0.024	0.031
b2	0.60	0.90	0.024	0.035
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.30	3.70	0.130	0.146
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	1.00	2.80	0.039	0.110
Ø P	3.00	3.40	0.118	0.134
ECN: E20-0684-Rev. D, 28-Dec-2020 DWG: 6021				



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