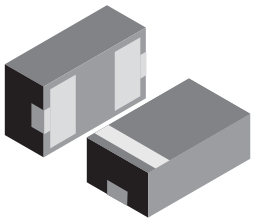
# ESD Protection Diode in LLP1006-2L



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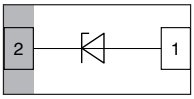


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## FEATURES

- Ultra compact LLP1006-2L package
- Low package height < 0.4 mm
- 1-line ESD protection
- Low leakage current < 1 µA
- Low load capacitance $C_D$ = 76 pF ($V_R$ = 2.5 V; f = 1 MHz)
- ESD immunity acc. IEC 61000-4-2
  ± 30 kV contact discharge
  ± 30 kV air discharge
- High surge current acc. IEC 61000-4-5 $I_{PP}$ > 16 A
- Soldering can be checked by standard vision inspection. No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e4
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

## MARKING (example only)

21121

Bar = cathode marking
X = date code
Y = type code (see table below)

## DESIGN SUPPORT TOOLS

click logo to get started

3D Models Available

| ORDERING INFORMATION | | | |
|---|---|---|---|
| DEVICE NAME | ORDERING CODE | TAPED UNITS PER REEL (8 mm TAPE on 7" REEL) | MINIMUM ORDER QUANTITY |
| VESD05A1A-HD1 | VESD05A1A-HD1-GS08 | 8000 | 8000 |

| PACKAGE DATA | | | | | | |
|---|---|---|---|---|---|---|
| DEVICE NAME | PACKAGE NAME | TYPE CODE | WEIGHT | MOLDING COMPOUND FLAMMABILITY RATING | MOISTURE SENSITIVITY LEVEL | SOLDERING CONDITIONS |
| VESD05A1A-HD1 | LLP1006-2L | H | 0.72 mg | UL 94 V-0 | MSL level 1 (according J-STD-020) | Peak temperature max. 260 °C |

| ABSOLUTE MAXIMUM RATINGS VESD05A1A-HD1 | | | | |
|---|---|---|---|---|
| PARAMETER | TEST CONDITIONS | SYMBOL | VALUE | UNIT |
| Peak pulse current | Acc. IEC 61000-4-5; $t_P$ = 8/20 µs; single shot | $I_{PPM}$ | 16 | A |
| Peak pulse power | Acc. IEC 61000-4-5; $t_P$ = 8/20 µs; single shot | $P_{PP}$ | 192 | W |
| ESD immunity | Contact discharge acc. IEC 61000-4-2; 10 pulses | $V_{ESD}$ | ± 30 | kV |
| | Air discharge acc. IEC 61000-4-2; 10 pulses | | ± 30 | kV |
| Operating temperature | Junction temperature | $T_J$ | -40 to +125 | °C |
| Storage temperature | | $T_{stg}$ | -55 to +150 | °C |

**PATENT(S): www.vishay.com/patents**
**This Vishay product is protected by one or more United States and international patents.**


For technical questions, contact: ESDprotection@vishay.com
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| **ELECTRICAL CHARACTERISTICS VESD05A1A-HD1** ($T_{amb}$ = 25 °C, unless otherwise specified) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **TEST CONDITIONS/REMARKS** | **SYMBOL** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| Protection paths | Number of lines which can be protected | $N_{channel}$ | - | - | 1 | lines |
| Reverse stand off voltage | Max. reverse working voltage | $V_{RWM}$ | - | - | 5 | V |
| Reverse voltage | At $I_R$ = 1 µA | $V_R$ | 5 | - | - | V |
| Reverse current | At $V_R$ = 5 V | $I_R$ | - | < 0.1 | 1 | µA |
| Reverse breakdown voltage | At $I_R$ = 1 mA | $V_{BR}$ | 6 | 6.8 | 7.5 | V |
| Reverse clamping voltage | At $I_{PP}$ = 1 A | $V_C$ | - | 7.2 | 8.5 | V |
| | At $I_{PP}$ = $I_{PPM}$ = 16 A | $V_C$ | - | 10.5 | 12 | V |
| Forward clamping voltage | At $I_{PP}$ = 1 A | $V_F$ | - | 1 | 1.5 | V |
| | At $I_{PP}$ = $I_{PPM}$ = 16 A | $V_F$ | - | 3.2 | 4.5 | V |
| Capacitance | At $V_R$ = 0 V; f = 1 MHz | $C_D$ | - | 130 | 150 | pF |
| | At $V_R$ = 2.5 V; f = 1 MHz | $C_D$ | - | 76 | - | pF |

**BiAs-MODE** (bidirectional asymmetrical protection mode)

With the VESD05A1A-HD1 one signal- or data-lines (L1) can be protected against voltage transients. With pin 1 connected to ground and pin 2 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage ($V_{RWM}$) the protection diode between data line and ground offers a high isolation to the ground line. The protection device behaves like an open switch.
As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage ($V_C$) is defined by the breakthrough voltage ($V_{BR}$) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.
Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage ($V_F$) clamps the negative transient close to the ground level.
Due to the different clamping levels in forward and reverse direction the VESD05A1A-HD1 clamping behaviour is bidirectional and asymmetrical (BiAs).

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**TYPICAL CHARACTERISTICS** ($T_{amb}$ = 25 °C, unless otherwise specified)

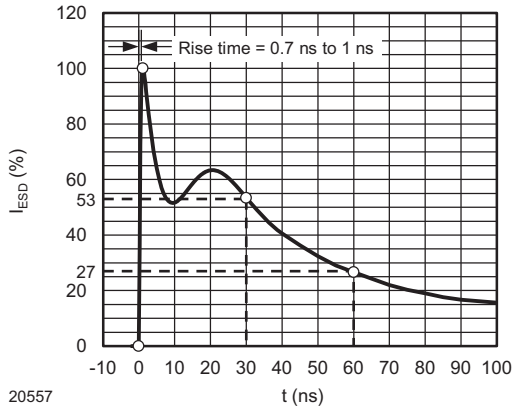


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

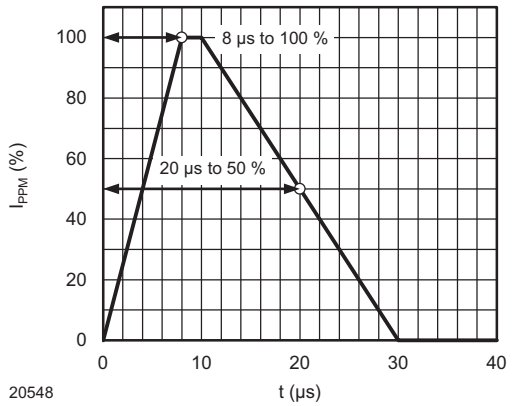


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form (acc. IEC 61000-4-5)

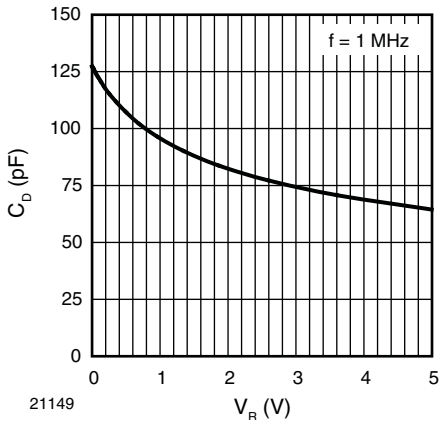


Fig. 3 - Typical Capacitance $C_D$ vs. Reverse Voltage $V_R$

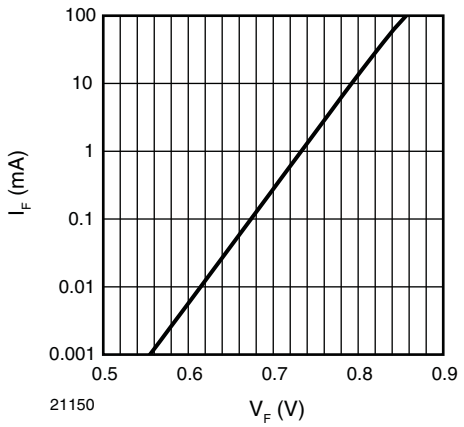


Fig. 4 - Typical Forward Current $I_F$ vs. Forward Voltage $V_F$

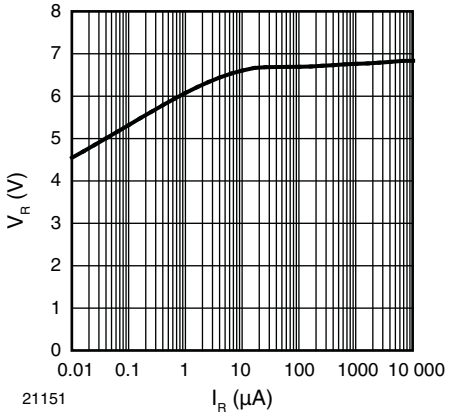


Fig. 5 - Typical Reverse Voltage $V_R$ vs. Reverse Current $I_R$

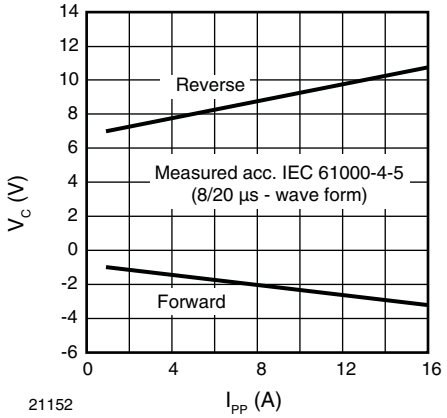


Fig. 6 - Typical Clamping Voltage vs. Peak Pulse Current $I_{PP}$


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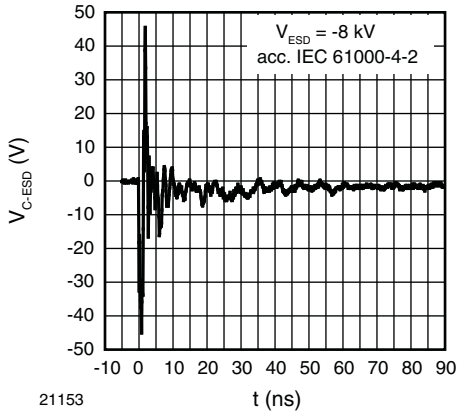


Fig. 7 - Typical Clamping Performance on - 8 kV ESD Events (acc. IEC 61000-4-2)

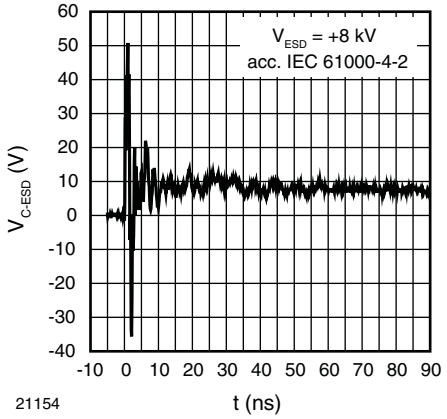


Fig. 8 - Typical Clamping Performance on + 8 kV ESD Events (acc. IEC 61000-4-2)

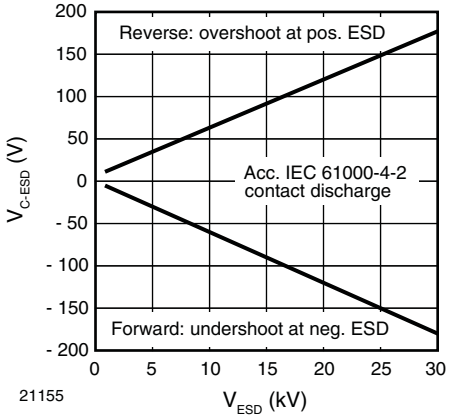


Fig. 9 - Typical max. Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)


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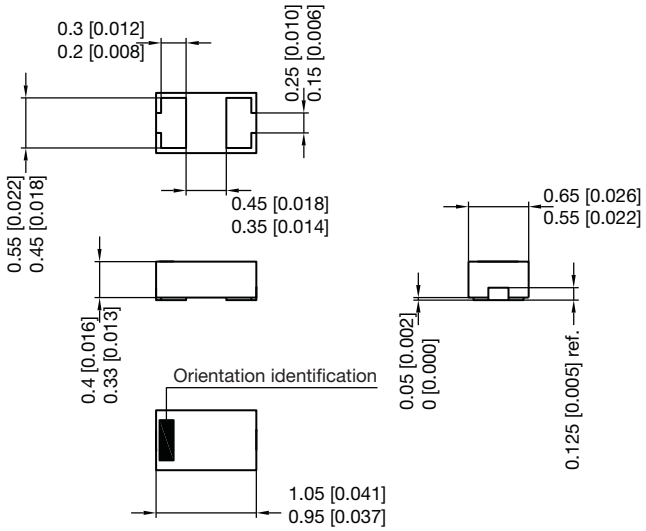
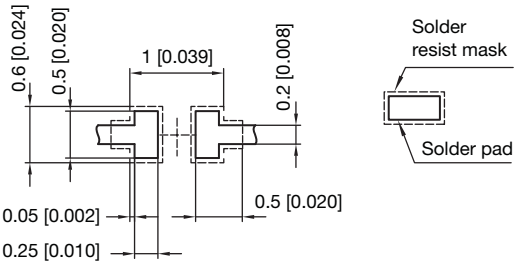
**PACKAGE DIMENSIONS** in millimeters (inches): **LLP1006-2L**




Foot print recommendation:




Pad Design Patented:
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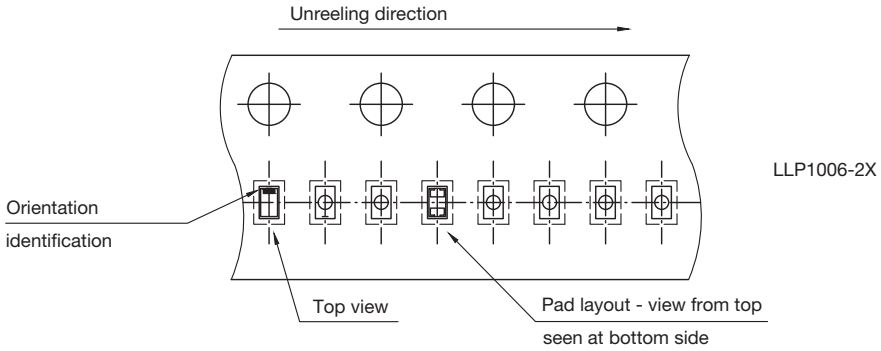


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