

Dual N-Channel 25 V (D-S) MOSFETs

DESCRIPTION

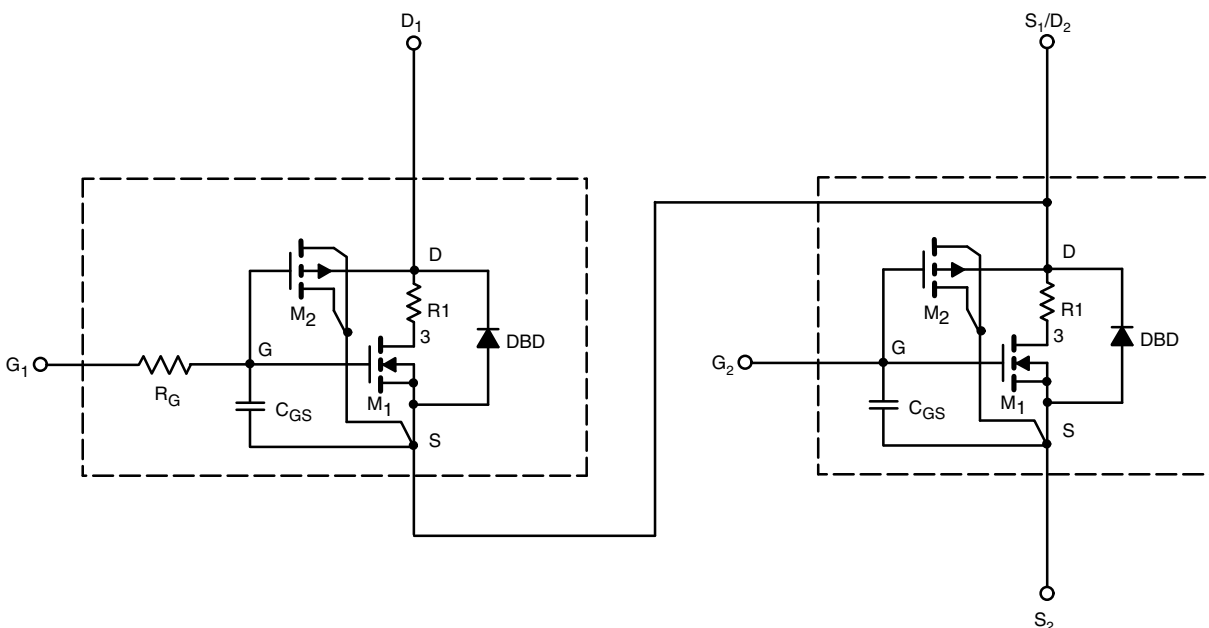
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT		
Static								
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.7	-	V		
			Ch-2	1.7	-			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A	Ch-1	0.00390	0.00380	Ω		
		V _{GS} = 10 V, I _D = 8 A	Ch-2	0.00179	0.00173			
		V _{GS} = 4.5 V, I _D = 3 A	Ch-1	0.00660	0.00640			
		V _{GS} = 4.5 V, I _D = 5 A	Ch-2	0.00281	0.00265			
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 5 A	Ch-1	29	40	S		
		V _{DS} = 10 V, I _D = 8 A	Ch-2	57	55			
Diode Forward Voltage ^b	V _{SD}	I _S = 5 A, V _{GS} = 0 V	Ch-1	0.80	0.81	V		
		I _S = 8 A, V _{GS} = 0 V	Ch-2	0.77	0.77			
Dynamic ^b								
Input Capacitance	C _{iss}	Channel-1 V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz Channel-2 V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	931	925	pF		
Output Capacitance	C _{oss}		Ch-2	2160	2150			
			Ch-1	321	310			
Reverse Transfer Capacitance	C _{rss}		Ch-2	779	800			
		Ch-1	58	52				
Total Gate Charge	Q _g	Channel-1 V _{DS} = 10 V, V _{GS} = 10 V, I _D = 5 A	Ch-1	12.1	12.5	nC		
			Ch-2	27	27			
		Channel-2 V _{DS} = 10 V, V _{GS} = 10 V, I _D = 8 A	Ch-1	5.6	5.9			
			Ch-2	12.3	12.5			
			Gate-Source Charge	Q _{gs}	Ch-1		2.5	2.5
					Ch-2		5.4	5.4
Gate-Drain Charge	Q _{gd}	Channel-2 V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 8 A	Ch-1	1.2	1.2			
			Ch-2	2.1	2.1			

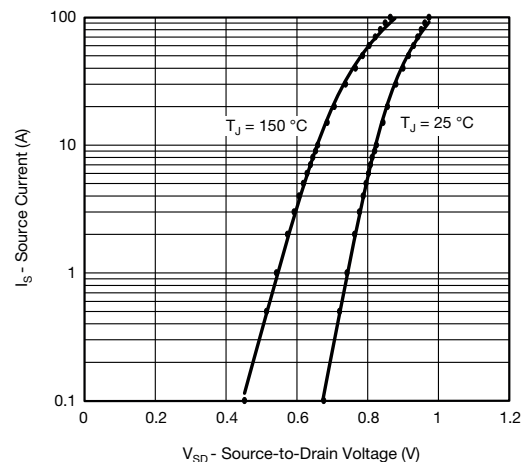
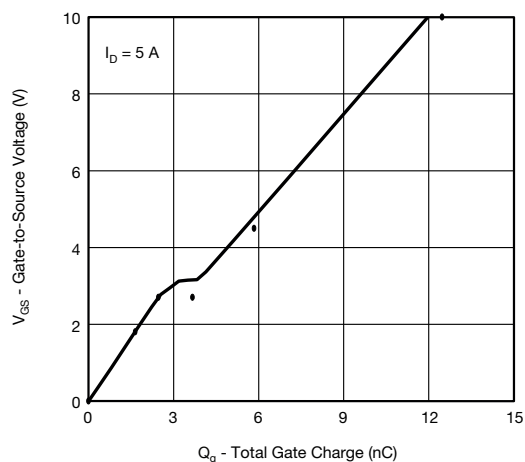
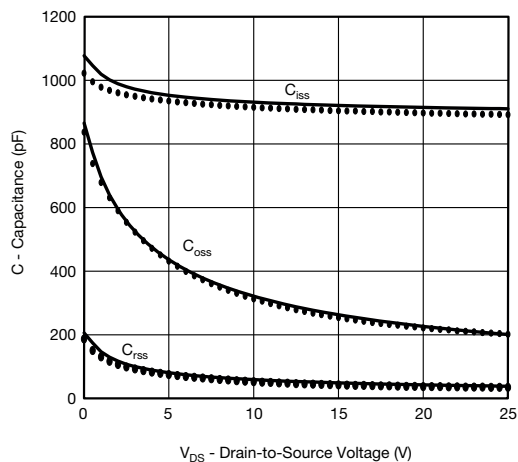
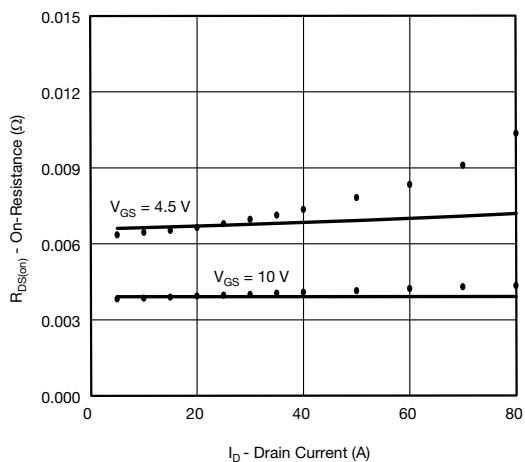
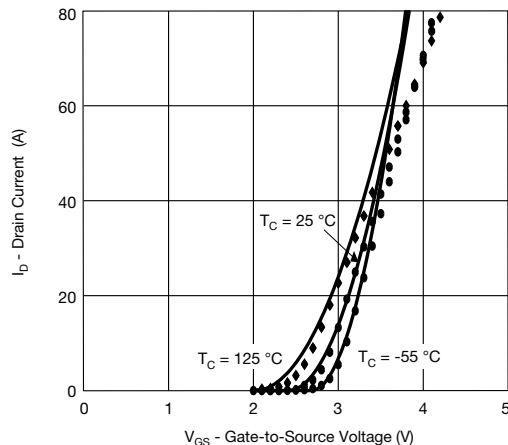
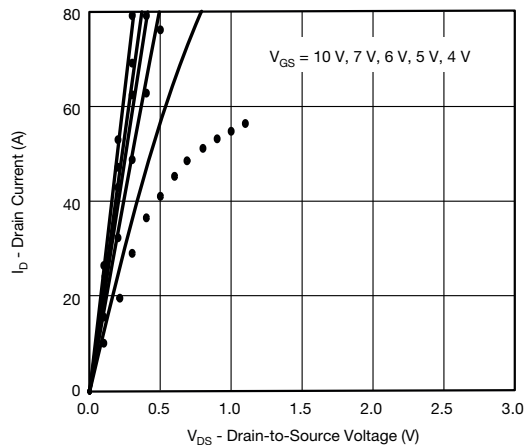
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$
b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$, unless otherwise noted

N-Channel 1 MOSFET



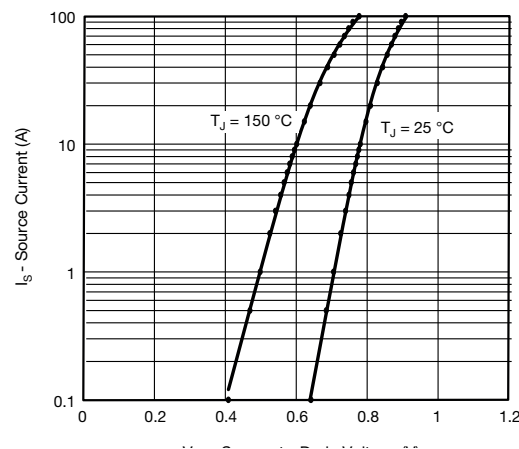
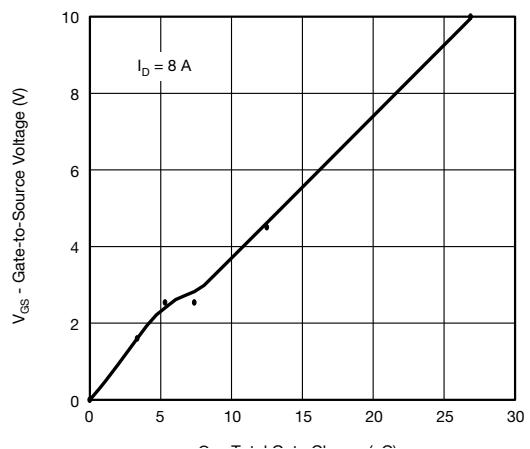
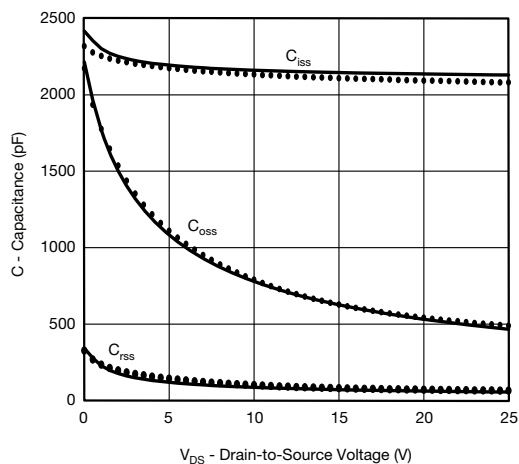
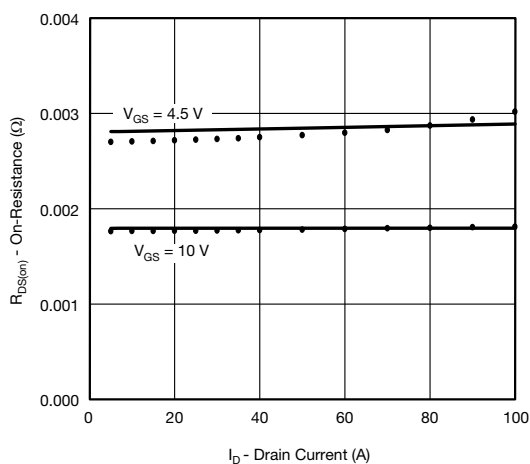
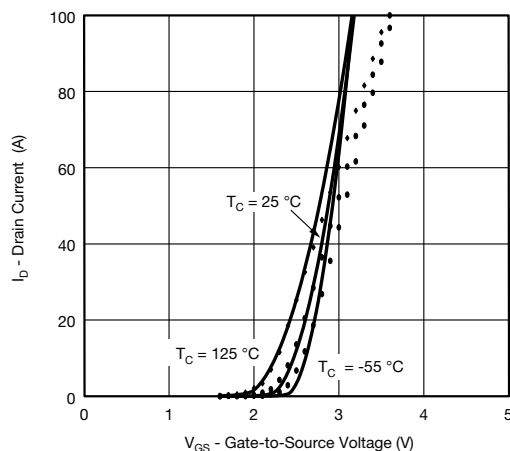
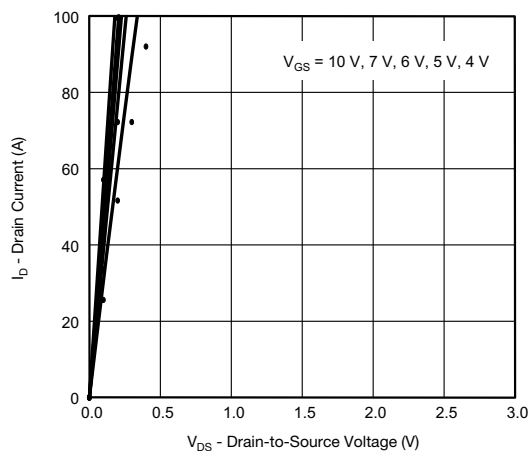
Note

- Dots and squares represent measured data



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$, unless otherwise noted

N-Channel 2 MOSFET



Note

- Dots and squares represent measured data

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