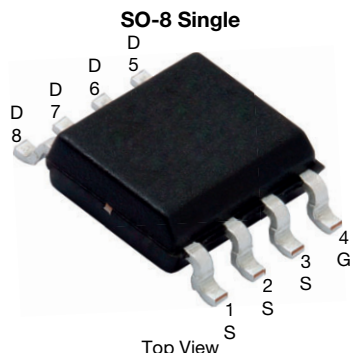


P-Channel 30 V (D-S) MOSFET



FEATURES

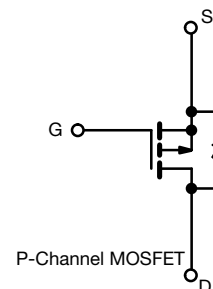
- TrenchFET® Gen IV p-channel power MOSFET
- 100% R_g tested
- Material categorization; for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Adapter switch
- Battery management
- Circuit protection
- Load switch
- Motor drive control



PRODUCT SUMMARY

V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0095
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0160
Q_g typ. (nC)	13
I_D (A) ^a	-18.3
Configuration	Single

ORDERING INFORMATION

Package	SO-8
Lead (Pb)-free and halogen-free	Si4425FDY-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	-20 / +16	V
Continuous drain current ($T_J = 150$ °C)	I_D	-18.3	A
	I_D	-14.7	
	I_D	-12.7 ^{b, c}	
	I_D	-10.2 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	-70	A
Continuous source-drain diode current	I_S	-4	A
	I_S	-1.9 ^{b, c}	
Single pulse avalanche current	I_{AS}	15	mJ
Single pulse avalanche energy	E_{AS}	11.25	
Maximum power dissipation	P_D	4.8	W
	P_D	3.1	
	P_D	2.3 ^{b, c}	
	P_D	1.5 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, d}	R_{thJA}	42	53	°C/W
Maximum junction-to-case (drain)	R_{thJF}	21	26	°C/W

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is 90 °C/W
- $T_C = 25$ °C



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-30	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-13	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1	-	-2.2	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = -20 V / +16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = 10 V	-10	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -10 A	-	0.0077	0.0095	Ω
		V _{GS} = -4.5 V, I _D = -10 A	-	0.0127	0.0160	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -10 A	-	47	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	-	1620	-	pF
Output capacitance	C _{oss}		-	250	-	
Reverse transfer capacitance	C _{rss}		-	56	-	
Total gate charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -10 A	-	27	41	nC
		V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -10 A	-	13	20	
Gate-source charge	Q _{gs}	V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -10 A	-	5.4	-	
Gate-drain charge	Q _{gd}		-	4.3	-	
Gate resistance	R _g	f = 1 MHz	4	10	17	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 1.5 Ω, I _D ≅ -10 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	22	44	ns
Rise time	t _r		-	48	96	
Turn-off delay time	t _{d(off)}		-	29	58	
Fall time	t _f		-	23	46	
Turn-on delay time	t _{d(on)}	V _{DD} = -15 V, R _L = 1.5 Ω, I _D ≅ -10 A, V _{GEN} = -10 V, R _g = 1 Ω	-	8	18	
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	42	84	
Fall time	t _f		-	22	44	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-4	A
Pulse diode forward current	I _{SM}		-	-	-70	
Body diode voltage	V _{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.78	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -10 A, di/dt = 100 A/μs, T _J = 25 °C	-	26	52	ns
Body diode reverse recovery charge	Q _{rr}		-	12	24	nC
Reverse recovery fall time	t _a		-	12	-	ns
Reverse recovery rise time	t _b		-	14	-	

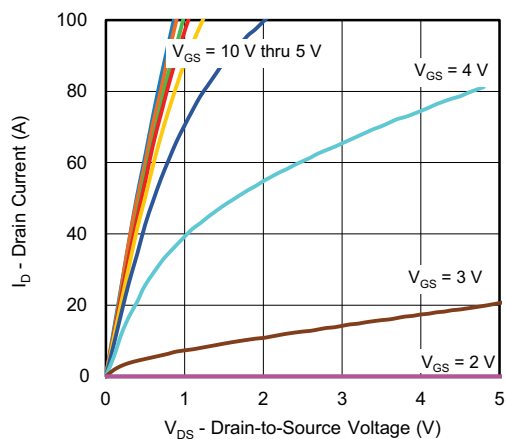
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

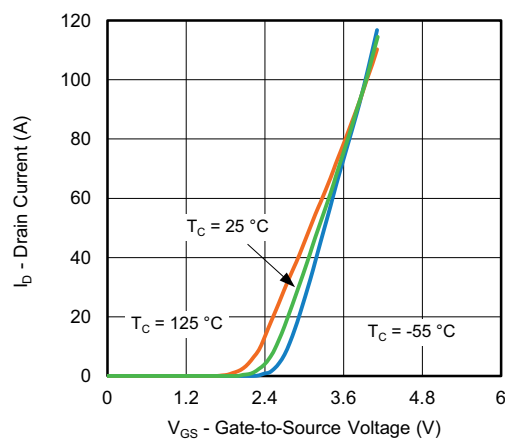
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



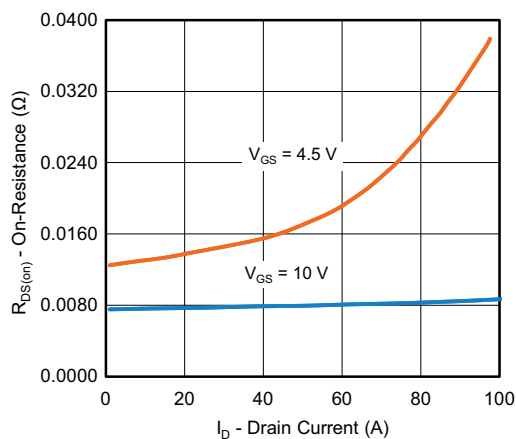
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



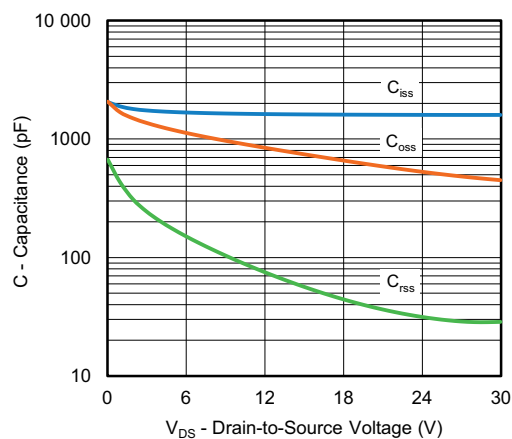
Output Characteristics



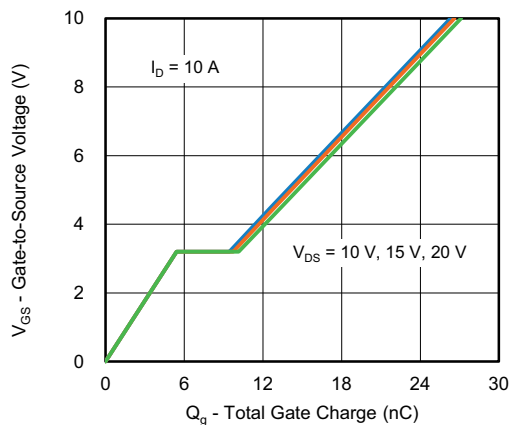
Transfer Characteristics



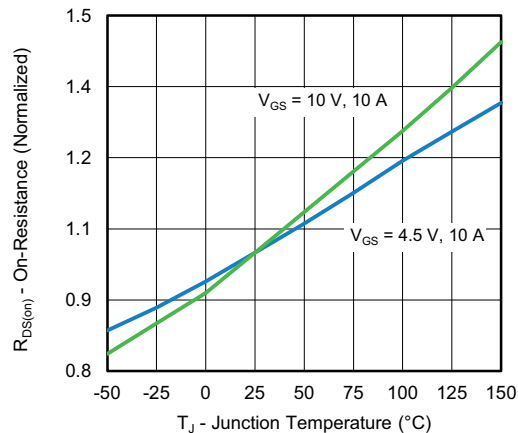
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



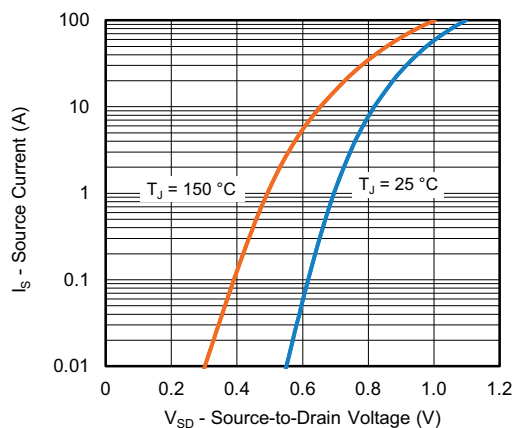
Gate Charge



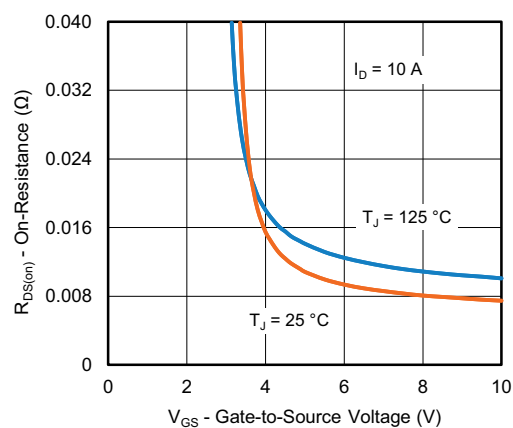
On-Resistance vs. Junction Temperature



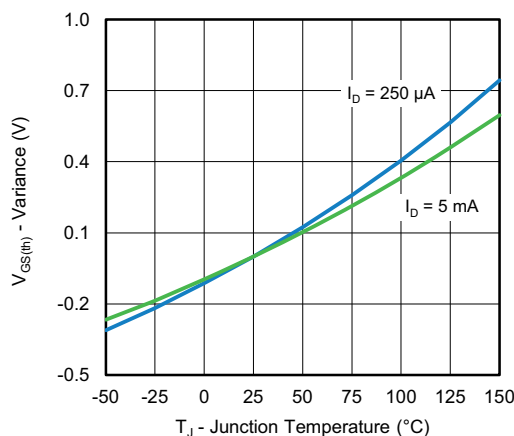
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



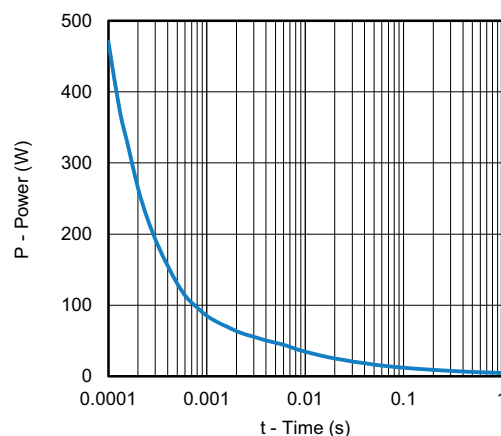
Source-Drain Diode Forward Voltage



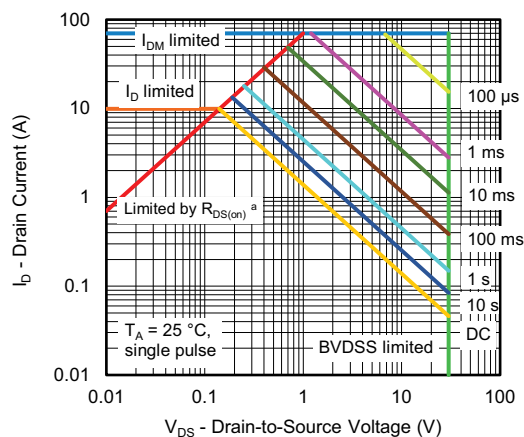
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



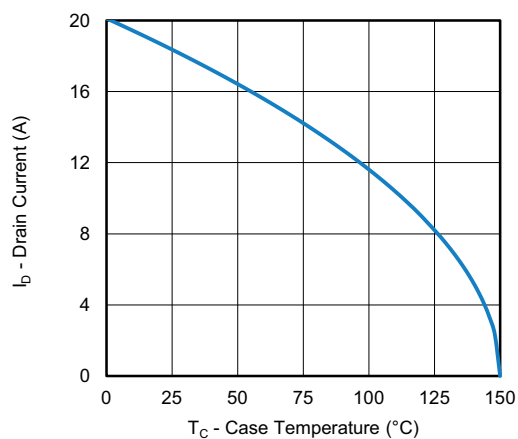
Safe Operating Area, Junction-to-Ambient

Note

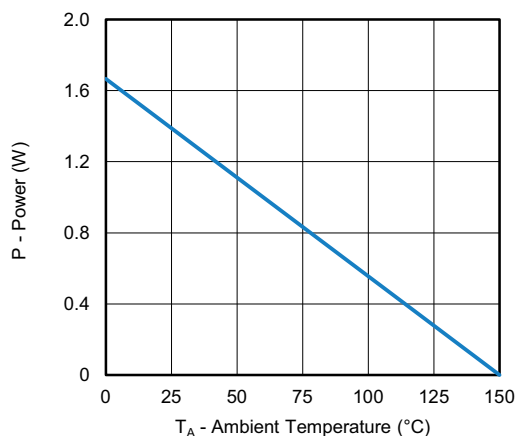
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



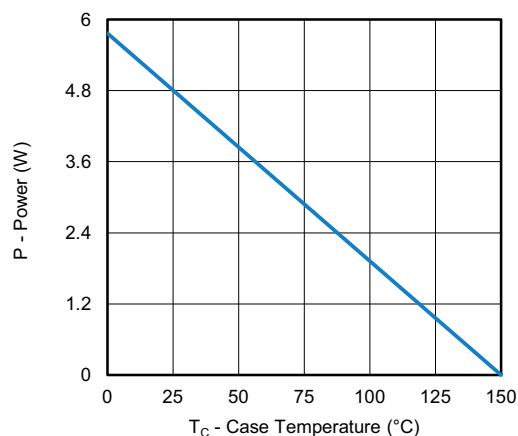
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Ambient



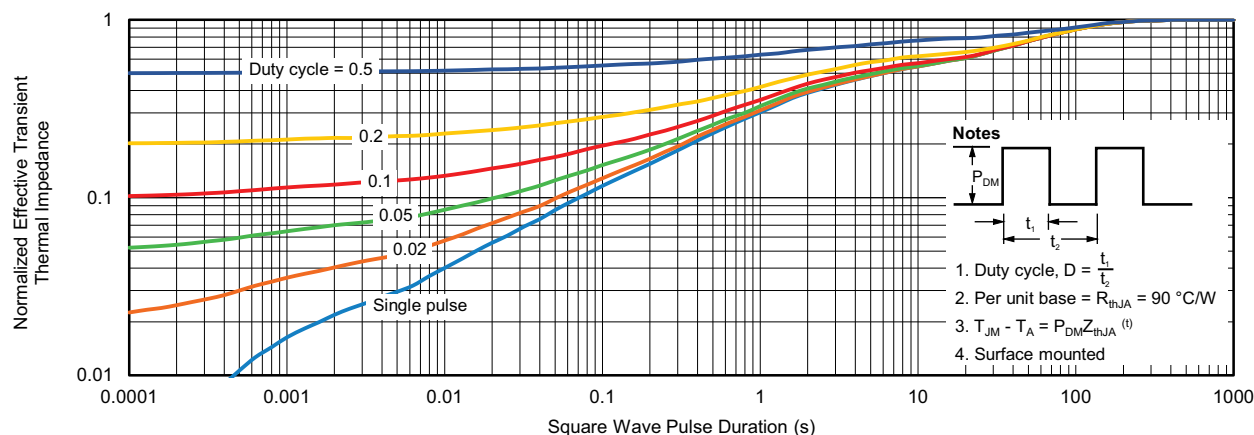
Power, Junction-to-Case

Note

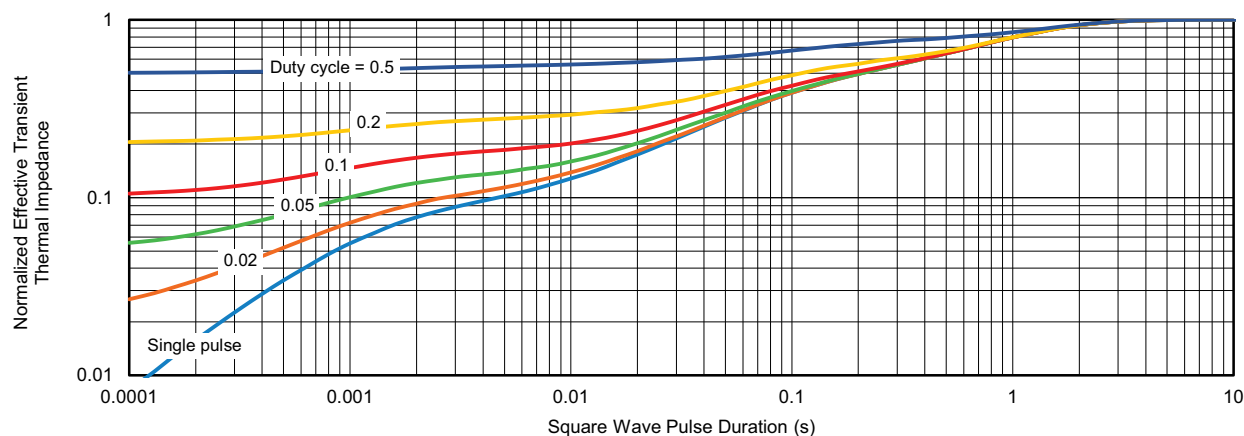
- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

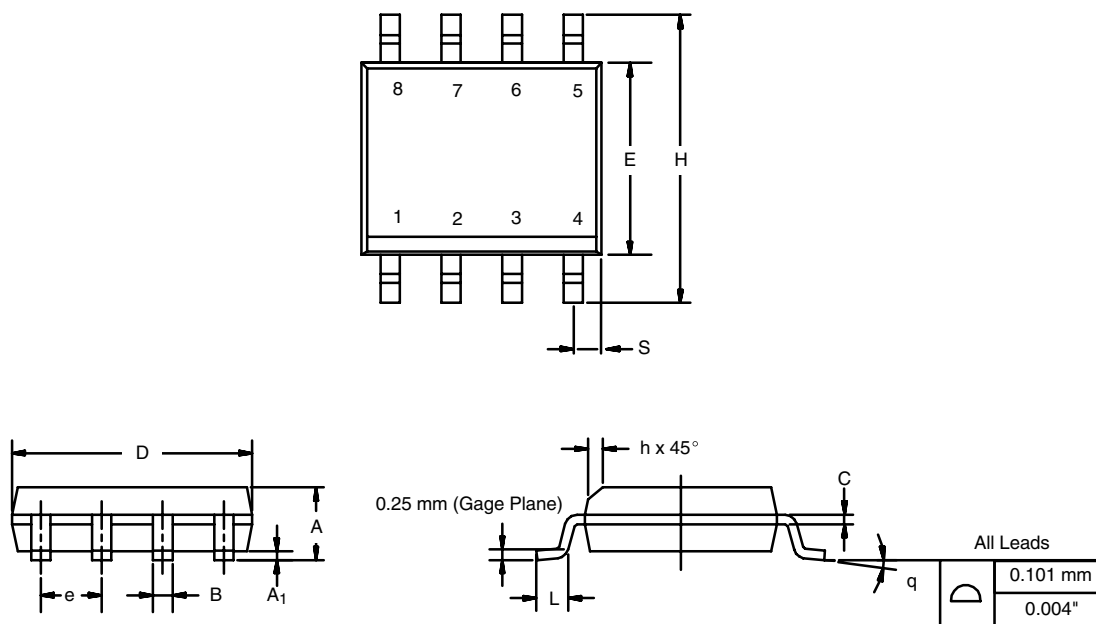


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77095.

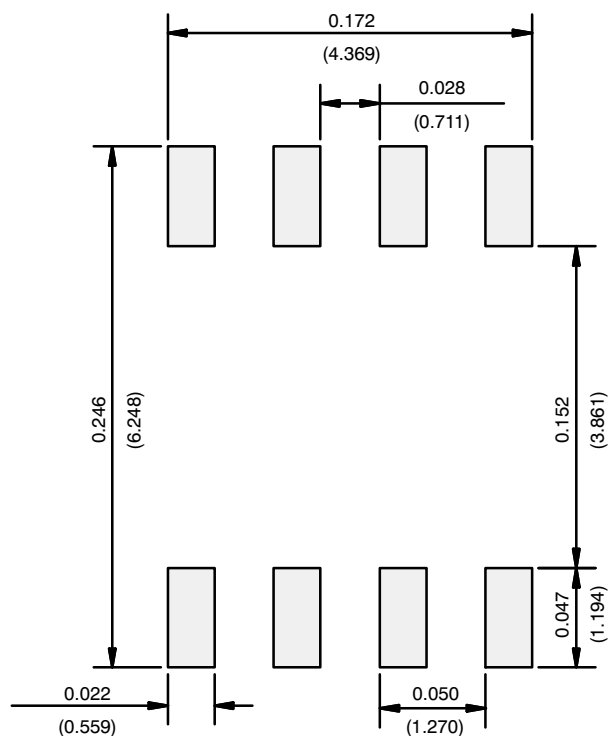
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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